1. A substrate carrier for securing semiconductor substrates, comprising:

a cassette having

an upper substrate entrance.

a lower substrate support opening.

a first side panel having an inner surface thereof, a train of parallel substrate support channels, said support channels having a bottom surface, a left side surface and a right side surface, said left and right side surfaces are perpendicular to said bottom surface.

a second side panel opposite said first side panel, having, on an inner surface a matching train of parallel substrate support channels;

an arcuate curbing member. disposed on a left side surface in each of said channels, and including

a top end having a sloped segment facing said entrance of said cassette permitting a substrate to slide by a necked portion of said substrate support channel, provided by said sloped segment, into a stepped bottom, therein securing said substrate.

2. The substrate carrier according to claim 1 wherein said upper entrance and said lower cassette support opening are formed by said first and second side panels while fixed apart by two end panels.

3. The substrate carrier according to claim 1 wherein said substrate support

channel surfaces are planar.

4. The substrate carrier according to claim 1 wherein said shape of curbing member restricts said substrates from jutting towards said substrate entrance.

5. The substrate carrier according to claim 1 wherein all the substrate support channels defined by the substrate size are spaced from immediately adjacent substrates at equal distances.

6. The substrate carrier according to claim 1 wherein said substrate support channels are configured to hold substrates in a vertical orientation.

7. The substrate carrier according to claim 1 wherein said parallel and perpendicular surfaces of said substrate support channels provides stress free containment of a fragile substrate by providing substrate freedom of movement within the cassette while preventing said substrate from jutting forward past said curbing member.

8. The substrate carrier according to claim 7 wherein said substrate support channels having a shape of three perpendicular surfaces prevents substrate chipping and breaking of highly stressed substrate edges.

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9. The substrate carrier according to claim 1 wherein said stepped bottom of said arcuate curbing member is placed so that said substrate does not jut out beyond the top edge of said cassette.

50 10. The substrate carrier according to claim 1 wherein an edge of said sloped profile is determined to permit the substrate freedom to move laterally to the limit provided by an offset dimension which is the difference of the lateral offset and the substrate diameter.

55 11. A wafer carrier for securing semiconductor wafers, comprising:

a cassette having

an upper wafer entrance.

a lower wafer support opening.

a first side panel having an inner surface thereof, a train of parallel

60 wafer support channels, said support channels having a bottom surface, a left side surface and a right side surface, said left and right side surfaces are perpendicular to said bottom surface.

a second side panel opposite said first side panel, having, on an inner surface a matching train of parallel wafer support channels;

65 an arcuate curbing member. disposed on a left side surface in each of said channels, and including

a top end having a sloped segment facing said entrance of said cassette permitting a wafer to slide by a necked portion of said wafer support channel, provided by said sloped segment, into a stepped bottom, therein securing said wafer.

12. The wafer carrier according to claim 11 wherein said upper entrance and said lower cassette support opening are formed by said first and second side panels while fixed apart by two end panels.

13. The wafer carrier according to claim 11 wherein said wafer support channel surfaces are planar.

14. The wafer carrier according to claim 11 wherein said shape of curbing member restricts said wafers from jutting towards said wafer entrance.

15. The wafer carrier according to claim 11 wherein all the wafer support channels defined by the wafer size are spaced from immediately adjacent wafers at equal distances.

16. The wafer carrier according to claim 11 wherein said wafer support channels are configured to hold wafers in a vertical orientation.

17. The wafer carrier according to claim 11 wherein said parallel and perpendicular surfaces of said wafer support channels provides stress free containment of a fragile wafer by providing wafer freedom of movement within the cassette while preventing said wafer from jutting forward past said curbing member.

18. The wafer carrier according to claim 17 wherein said wafer support channels having a shape of three perpendicular surfaces prevents wafer chipping and breaking of highly stressed wafer edges.

19. The wafer carrier according to claim 11 wherein said stepped bottom of said arcuate curbing member is placed so that said wafer does not jut out beyond the top edge of said cassette.

20. The wafer carrier according to claim 11 wherein an edge of said sloped profile is determined to permit the wafer freedom to move laterally to the limit provided by an offset dimension which is the difference of the lateral offset and the wafer diameter.

21. A method for protecting semiconductor wafers in a wafer carrier, comprising the steps of:

providing a cassette having

an upper wafer entrance.

a lower wafer support opening.

a first side panel having an inner surface thereof, a train of parallel wafer support channels, said support channels having a bottom surface, a left side surface and a right side surface, said left and right side surfaces are perpendicular to said bottom surface.

a second side panel opposite said first side panel, having, on an inner surface a matching train of parallel wafer support channels;

an arcuate curbing member. disposed on a left side surface in each of said channels, and including

a top end having a sloped segment facing said entrance of said cassette permitting a wafer to slide by a necked portion of said wafer support channel, provided by said sloped segment, into a stepped bottom, therein securing said wafer.

22. A method according to claim 21 wherein said upper entrance and said lower cassette support opening providing liquid chemical access to all surfaces of contained wafers .

23. A method according to claim 21 wherein said wafer support channel surfaces are planar thereby permitting unrestrained freedom of the wafers

during wet processes and during handling.

24. A method according to claim 21 wherein said shape of curbing member restricts said wafers from jutting towards said wafer entrance during handling.

25. A method according to claim 21 wherein all the wafer support channels defined by the wafer size are spaced from immediately adjacent wafers at equal distances.

26. A method according to claim 21 wherein said wafer support channels are configured to hold wafers in a vertical orientation.

27. A method according to claim 21 wherein said parallel and perpendicular surfaces of said wafer support channels provides stress free containment of a fragile wafer by providing wafer freedom of movement within the cassette while preventing said wafer from jutting forward past said curbing member.

28. A method according to claim 7 wherein said wafer support channels having a shape of three perpendicular surfaces prevents wafer chipping and breaking of highly stressed wafer edges.

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29. A method according to claim 21 wherein said stepped bottom of said arcuate curbing member is placed so that said wafer does not jut out beyond the top edge of said cassette.

30. A method according to claim 21 wherein an edge of said sloped

160 profile is determined to permit the wafer freedom to move laterally to the limit provided by an offset dimension which is the difference of the lateral offset and the wafer diameter.